ERIC DAVID WALLIN

I am primarily a digital designer for reprogrammable logic devices (i.e. FPGAs and CPLDs made by Xilinx, Altera, and Lattice) with side experience in mixed signal and analog design. Although I prefer Verilog HDL, I am equally fluent in VHDL and have many years of experience with both. My desire is to do HDL work on projects that involve music in some way, and I would prefer not to work on ASICs or anything defense related.

I have designed many types of digital structures targeted towards programmable logic including DPLLs, stack processors, TSIs, UARTs, I2C & SPI masters / slaves / arbiters, UTOPIA interfaces, generic FIFOs as well as Ethernet packet and ATM cell FIFOs, watchdog timers, and processor register sets with local bus bridges. My designs are extensively documented and I strive for high levels of readability, portability, and craftsmanship.

EMPLOYMENT

Member of Technical Staff **Alcatel-Lucent, Whippany NJ.** **1998 to 2009**

I architected, designed, and implemented the main packet buffer on an eight line GPON Line Termination (GLT8) unit, including a pool of linked lists maintained in FPGA BRAM and external DDR2 and QDR. Previous to that I implemented the packet processing sections of several flavors of GPON Multi Dwelling Units (MDUs) including VDSL and gigabit Ethernet variants. I also coded the low-level CPLDs on those units.

I had a major HLD hand in three telecom product lines: AnyMedia, Stinger, and MMAP. These are DLC (Digital Loop Carrier) and DSLAM (Digital Subscriber Line Access Multiplexer) systems which consist of multiple card cage / backplane combinations, several flavors of system controller cards, and a large variety of trunk and subscriber line interface cards.

Often I was responsible for system timing - the specification and design of solutions that include the use of PLLs and DPLLs - and depend on analysis tools that I have written for this. My VHDL DPLL is used for system timing on the Stinger IP2100 controller card; it replaced a more expensive, inferior discrete vendor part. I have performed extensive jitter & wander compliance tests on my designs, and have written compliance documents for an SDSL line card and several OC3 trunk / controller cards.

Circuit Design Consultant **University of Virginia, Charlottesville, VA.** **1997**

Designed and implemented a prototype mid-infrared LED / thin film sensor spectrometry-based CO_2 detector for a project funded by the Virginia Patent Foundation. This was a mixed analog / digital design.

Various **American GFM, Chesapeake, VA.** **1985 to 1993**

As an **Assistant Mechanical Engineer** I interacted with engineers from aerospace firms, performed experiments on customer materials and blades in our ultrasonic cutting lab, fielded customer inquiries, and wrote the programming and maintenance manuals for these machines. In my role as **CNC Programmer** I programmed three and four axis vertical and horizontal CNC milling machines, as well as a metal plate torch cutter. I was responsible for choice of tooling, setups, and design and manufacture of any necessary fixtures. As a **CNC Machinist** I operated three-axis vertical mill on a wide variety of jobs, mostly short-run, close tolerance work. Finally, as a **QA Inspector** I inspected manufactured parts using three-axis computer controlled validators, micrometers, gauges, etc.

EDUCATION

MSEE **University of Virginia, Charlottesville, VA.** **August 1998**

Thesis: ISOTACH: Hardware Acceleration of High Speed Networks for Isochronous Multi-computing *-and-* Recirculated Delta Sigma Modulated Bitstreams for Music Synthesis in Reconfigurable Hardware. GPA 4.00/4

BSEE **University of Virginia, Charlottesville, VA.** **May 1996**

Concentration areas: Communications, Control Systems, Power Electronics. Thesis: Discrete-Time Pulse Waveforms for Three Phase Power Inverters. GPA 3.78/4

PUBLICATIONS, PATENTS, ACADEMIC HONORS, PROFESSIONAL AFFILIATIONS

- *"An Optical Sensor for Gas Monitoring"* Proceedings of the ISDRS, 1997.
- *"Delta-Sigma Waveguides for Music Synthesis"* Computer Music Journal, Winter 1999, Vol.23, Issue 4.
- Patent Awarded: *In-Phase Alignment for PLLs.*
- My Graduate work fully funded my academic expenses, including a significant stipend.
- Recipient of the Old Crows Capitol Club full undergraduate scholarship in both 1995 and 1996.
- Received the 1996 Lewis T. Rader Award for academic excellence.
- IEEE; Gamma Pi chapter of HKN.